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(54) Semiconductor antifuse structure and method.

(57) A method for forming an array of antifuse structures on a semiconductor substrate which previously has had CMOS devices fabricated thereupon up to first metallization. A fuse structure is formed as a sandwich by successively depositing a bottom layer of TiW, a layer of amorphous silicon, and a top layer of TiW. The amorphous silicon is formed in an antifuse via formed in a dielectric layer covering the bottom layer of TiW. First metallization is deposited and patterned over the top layer of TiW. An intermetal dielectric layer is formed over the fuse array and second metal conductors are formed thereupon. An alternative embodiment includes forming an oxide sidewall spacer around the periphery of an antifuse structure. Connection resistance to the bottom layer of TiW is lowered by using a number of vias between the second-metal conductors and the bottom layer of TiW in a row of an array of antifuse devices.

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This invention relates to antifuse structures and methods for forming semiconductor antifuse structures.

An antifuse element is an electrically programmable device which is normally in an open-circuit, or high resistance, state. A programming signal changes an antifuse device to a low-resistance state. One type of antifuse is formed of high resistivity amorphous silicon which dramatically changes resistance upon application of an appropriate signal. The fusing mechanism is described as electrothermal switching. Once a critical value of an electric field is established across an amorphous or polycrystalline silicon film, a conductive filament having a relatively low resistance is formed in the film.

We will describe an antifuse structure which has reduced resistance and reduced capacitance.

We will describe an antifuse structure that is manufacturable with a CMOS process.

We will describe an antifuse structure which has lower resistance connections to the fuse structure itself.

We will describe an antifuse structure which permits use of a more controllable programming voltage by using amorphous silicon as a fuse material.

We will describe an antifuse structure which provides a tight packing density in any array configuration.

In the paper IEEE International Solid-State Circuits Conference 28 (1985) February, 32nd Conference, Coral Gables, Florida, U.S.A there is described an interconnection system which is deposited on a bare silicon wafer. The design is based on a four layer metallization process. The two lower layers facilitate power distribution and the two upper layers implement an array of uncommitted lines which can be linked to each other via antifuses. The antifuses, consisting of an amorphous silicon alloy, are sandwiched into insulation holes between the third and fourth metal layers. Eleven deposition and eight masking steps are needed. The ground plane is not patterned at all. Barrier metals are patterned together with the metal layer to which they are attached.

According to one aspect the present invention provides a method of forming an antifuse structure comprising the steps of:

providing a silicon substrate which has been processed with CMOS process steps through contact formation and which has circuit elements formed thereon;

forming a protective layer over the circuit elements;

masking and etching said protective layer away from a fuse area;

depositing a first layer of TiW over said fuse area;

depositing a layer of antifuse silicon material over said first layer of TiW;

depositing a second layer of TiW over said layer of antifuse silicon material;

masking and etching said first layer of TiW, said layer of antifuse silicon material, and said second layer of TiW to form a TiW-Si-TiW antifuse sandwich;

depositing an oxide layer and etching a sidewall spacer from said oxide layer around the periphery of said TiW-Si-TiW antifuse sandwich;

removing the protective layer;

depositing a layer of first conductor material over said second layer of TiW and over said circuit elements;

etching portions of the layer of the first conductor material and said second layer of TiW;

forming a planarized dielectric layer over said substrate;

forming a via mask and etching standard vias to said layer of first conductor material and etching pick-up vias to said first layer of TiW; and

depositing and etching a layer of a second conductor material over said planarized dielectric layer.

The present invention also provides an antifuse structure comprising:

a semiconductor substrate;

a first layer of TiW formed on said semiconductor substrate;

a layer of antifuse silicon formed on said first layer of TiW;

a second layer of TiW formed on said layer of antifuse silicon, said first and second layers of TiW and said layer of antifuse silicon forming a vertical antifuse sandwich structure;

a sidewall spacer formed adjacent to and surrounding the periphery of said antifuse sandwich structure;

a first metal layer overlying said sidewall spacer and said antifuse sandwich structures;

an intermetal dielectric layer formed over said first metal layer; and

a second metal connected to the first TiW layer through a via formed in said intermetal dielectric layer to provide reduced connection resistance to said first TiW layer.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention:

FIGURE 1 is a cross-sectional view of a semiconductor structure incorporating the invention.

FIGURES 2A and 2B are plan views of portions of an array of antifuses.

FIGURES 3A through 3D are cross-sectional views showing various stages in the formation of an antifuse according to the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to those embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. The structures described are formed using well known semiconductor fabrication techniques.

FIGURE 1 shows an antifuse structure 70 formed on a silicon semiconductor substrate 72 that has been processed through standard CMOS process steps up through contact formation. The antifuse structure 70 is fabricated as a sandwich structure. A first layer of TiW 76 is formed on the substrate. A layer 78 of preferably amorphous silicon or polysilicon is formed on the first layer of TiW 76. A second layer of TiW 80 is formed over the silicon layer 78. A silicon dioxide sidewall spacer 82 is formed to surround the periphery of the sandwich structure. A first metal, or conductive layer, 84 is formed over the top surface of the second layer of TiW 80 and the sidewall spacer 82. A standard intermetal dielectric layer 86 is formed over the first metal layer 84. A second metal aluminum layer 88 is formed and patterned over the standard dielectric layer 86. The second metal connects the first TiW layer through vias at regular intervals on a fuse array. The second TiW is removed between adjacent first metal lines as the first metal is patterned, thus forming self-aligned vertical fuse structures.

FIGURES 2A and 2B (in more detail) show partial plan views of some of the elements of a portion of an array of antifuse devices,

as shown in cross-section in FIGURE 1. A number of first-metal aluminum conductors (typically shown as 102a-102j) are formed as parallel strips with a certain pitch, or spacing, therebetween. Beneath the first metal conductors are formed antifuse structures (typically indicated as 104) each of which has a second layer of TiW beneath the first metal conductors. When the first metal aluminum layer is masked and etched, the TiW in the areas 106 between the antifuses 104 is also removed to leave only amorphous silicon areas 106 between the antifuses 104. This provides a row of self-aligned antifuses, spaced apart by the first metal pitch, as shown in the FIGURES. Additional rows of antifuses are located parallel to that row of antifuses. A second-metal aluminum conductor 108, crosses over and is perpendicular to the first metal conductors 102. A via 110 (typically shown) extends from the second metal conductors (typically shown as 108a-108f) to respective first layer of TiW at the bottom of the antifuse structure. The vias provide a plurality of connections between the second-metal conductor and the first TiW for a row of antifuse structures. This provides a reduced-resistance connection for the antifuse structures. Consequently, TiW is usable for the bottom conductor of the antifuses while still having lower connection resistances.

FIGURE 2A shows the vias 110 spaced apart every 5 antifuses, or 6 metal-one pitches. In the prior art, external connections, using metal-two conductors to the bottom TiW layer would be made only at an end of a bottom conductor line. Using TiW in that connection arrangement would result in higher resistance connections. Using a number of connection vias for second-metal connections, as indicated in the drawing significantly reduces the connection resistance to any one of the antifuse structures.

FIGURES 3A-3D show various process stages in the formation of an antifuse structure elements forming an array of antifuses similar to those shown in FIGURE 1.

FIGURE 3A shows a standard CMOS-processed wafer, processed up to first metallization. Over the surface of the substrate is then formed a protective layer 116 preferably 500-1000 Angstroms of TiW, or aluminum, to protect various previously formed circuit components and active devices formed on the substrate. A masking and etching step removes that portion of the protective layer 116 in the fuse area 118 in which a fuse structure is to be formed.

FIGURE 3B shows a first layer 120 of 2500 A of TiW deposited in the fuse area 118. A layer 122 of 1000-2000 A of amorphous or polysilicon is deposited over the TiW layer 120. A second layer 124 of 1000-2000 A of TiW is deposited on the layer 122. A masking and etching step is then used to etch the TiW layers 120,124 and the silicon layer 122 to form a vertical antifuse sandwich 126 as indicated in the drawing.

FIGURE 3C shows the fuse structure 126 with an oxide sidewall spacer 128 surrounding the periphery of the fuse structure. The sidewall spacer 128 is formed by a plasma oxide deposition over the fuse structure. A subsequent isotropic etching of the oxide layer produces the sidewall 128 as

shown. A photoresist mask is used to protect fuse structure as protective TiW is wet etched off of circuit elements. The wafer is now ready for standard first metallization.

FIGURE 3D shows a first-metallization layer of aluminum 138 deposited over the surface of the substrate. A barrier metal could be used if needed for CMOS circuit elements. A first metal masking and etching step etches away the aluminum 138 in the area 140 as shown to form the structure shown in FIGURE 3D. The TiW 124 is also etched during the aluminum 138 etch. The next steps are conventional in semiconductor fabrication. A planarized dielectric layer is then deposited over the surface of the substrate. A via masking and etching step then forms standard vias to the aluminum conductors and pick-up vias to the TiW layer 120. A standard second metallization step is then used.

There are some advantages of the method associated with the structure of FIGURES 1 and 3A-3D. The TiW-Si-TiW structure is planar and provides more uniform electric fields across an antifuse structure during programming. The bottom TiW not etched or damaged prior to Si deposition. The pitch, or spacing, of the fuse array elements is as dense as the pitch of the first metallization because of the self-alignment characteristic of the process described. The fuse and first metal are completely self-aligned. The circuit contacts are protected from all etching steps. Therefore, no change in the contact shape occurs.

Other barrier metals could be used, instead of TiW, for example, TiN or W. The protection layer over the circuit elements could be other metals such as aluminum.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.

Claims

1. A method of forming an antifuse structure comprising the steps of:

providing a silicon substrate (72) which has been processed with CMOS process steps through contact formation and which has circuit elements formed thereon;

forming a protective layer (116) over the circuit elements;

masking and etching said protective layer away from a fuse area (118);

depositing a first layer (120) of TiW over said fuse area;

depositing a layer (122) of antifuse silicon material over said first layer of TiW;

depositing a second layer (124) of TiW over said layer of antifuse silicon material;

masking and etching said first layer of TiW, said layer of antifuse silicon material, and said second layer of TiW to form a TiW-Si-TiW antifuse sandwich;

depositing an oxide layer and etching a sidewall spacer (128) from said oxide layer around the periphery of said TiW-Si-TiW antifuse sandwich;

removing the protective layer;

depositing a layer (138) of first conductor material over said second layer of TiW and over said circuit elements;

etching portions of the layer of the first conductor material and said second layer of TiW;

forming a planarized dielectric layer over said substrate;

forming a via mask and etching standard vias to said layer of first conductor material and etching pick-up vias to said first layer of TiW; and

depositing and etching a layer of a second conductor material over said planarized dielectric layer.

2. The method as claimed in claim 1 wherein said protective layer is a layer of TiW.

3. The method as claimed in claim 1 wherein said protective layer is aluminum.

4. The method as claimed in claim 1, 2 or 3 including the step of depositing a layer of a barrier metal prior to depositing the layer of first conductor material over circuit elements.

5. The method as claimed in any of claims 1 to 4 wherein said antifuse silicon is a layer of amorphous silicon.

6. An antifuse structure comprising:

a semiconductor substrate (72);

a first layer (120) of TiW formed on said semiconductor substrate;

a layer (122) of antifuse silicon formed on said first layer of TiW;

a second layer (124) of TiW formed on said layer of antifuse silicon, said first and second layers of TiW and said layer of antifuse silicon forming a vertical antifuse sandwich structure;

a sidewall spacer (128) formed adjacent to and surrounding the periphery of said antifuse sandwich structure;

a first metal layer (138) overlying said sidewall spacer and said antifuse sandwich structures;

an intermetal dielectric layer formed over said first metal layer; and

a second metal connected to the first TiW layer through a via formed in said intermetal dielectric layer to provide reduced connection resistance to said first TiW layer.

7. The antifuse structure as claimed in claim 6 wherein said layer of antifuse silicon includes a layer of amorphous silicon.

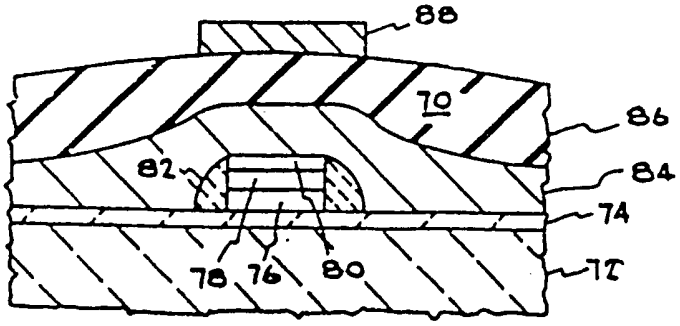

FIG. 1

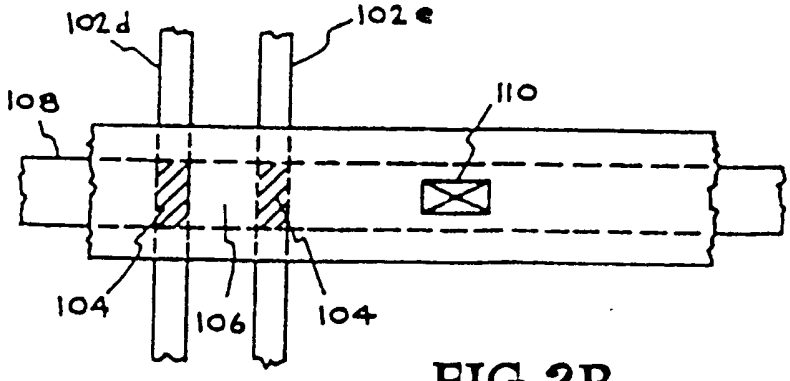

FIG. 2B

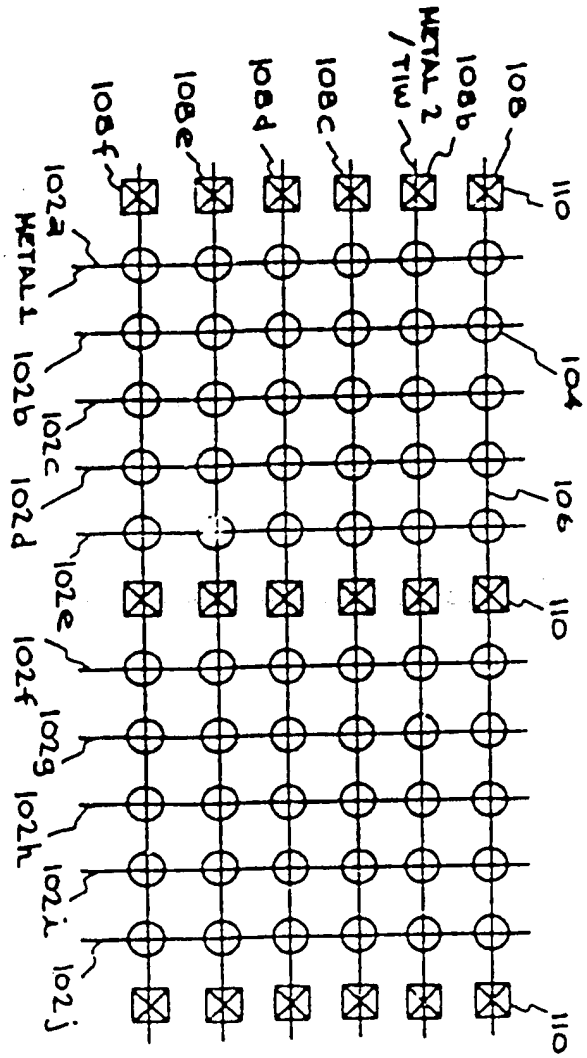
108f
108e
108d
108c
METAL 2 / TiW
108b
108
110
102a
METAL 1
102b
102c
102d
102e
102f
102g
102h
102i
102j
104
106
110
110

FIG. 2A

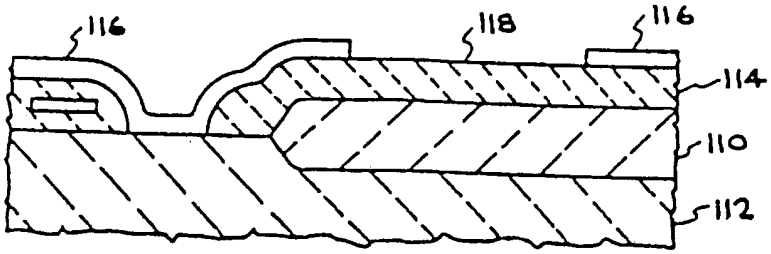

FIG.3A

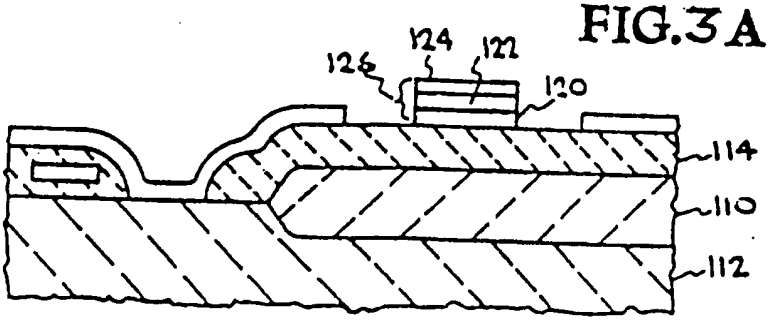

FIG.3B

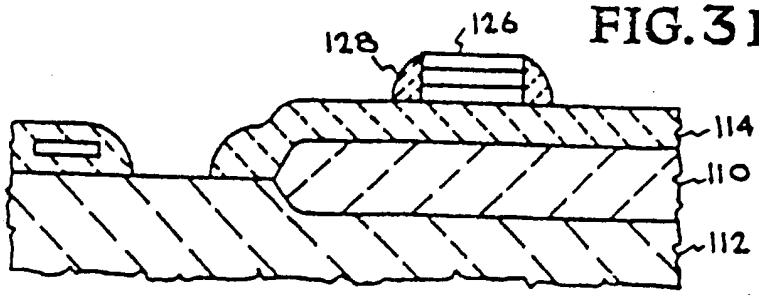

FIG.3C

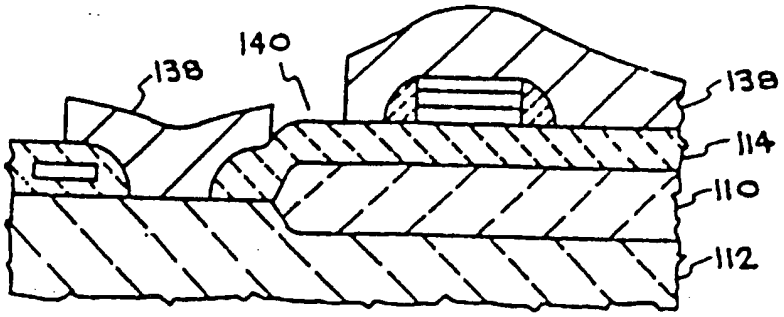

FIG.3D